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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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HUFFMAN LAW GROUP, P.C. 1832 N. CASCADE AVE. COLORADO SPRINGS, CO 80907-7449			MEONSKE, TONIA L	
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2183

DATE MAILED: 01/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/849,658	Applicant(s) HENRY ET AL.	
	Examiner Tonia L Meonske	Art Unit 2183	

-- Th MAILING DATE of this communication appears on the cover sheet with the corresponding address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 September 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-63 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-63 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-6, 10-15, 46-53, and 57-59, and 61-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiles et., US Patent 5,163,140, in view of Gochman et al., US Patent 5,964,868.

3. Claims 7, 54, 55, 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiles et., US Patent 5,163,140, in view of Gochman et al., US Patent 5,964,868 and Fite et al., US Patent 5,142,634.

4. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiles et., US Patent 5,163,140, in view of Gochman et al., US Patent 5,964,868 and Brown et al., US Patent 5,867,701.

5. The rejections to claims 1-15, 46-59, and 61-63 are respectfully maintained and incorporated by reference as set forth in the last office action, mailed on May 18, 2004.

6. Claim 16-33, 36-45 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiles et al., US Patent 5,163,140, in view of Gochman et al., US Patent 5,964.

7. Referring to claim 16, Stiles et al. have taught a microprocessor for detecting and correcting an erroneous speculative branch, comprising:

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- a. an instruction cache, for providing a line of instruction bytes selected by a fetch address, said fetch address provided to said instruction cache on an address bus (Figure 1, ICACHE RAMS, column 5, line 51-column 6, line 12);
 - b. a speculative branch target address cache (BTAC), coupled to said address bus, for providing a speculative target address of a previously executed branch instruction in response to said fetch address (column 9, lines 27-58);
 - c. control logic, coupled to said BTAC, configured to control a multiplexer to select said speculative target address as said fetch address during a first period whether or not said previously executed branch instruction is present in said line (column 9, lines 27-58, column 13, line 47-column 14, line 2); and
 - d. prediction check logic, coupled to said BTAC, configured to detect that said control logic controlled said multiplexer to select said speculative target address erroneously (column 6, line 59-column 7, line 30, column 16, lines 33-36);
 - e. wherein said control logic is further configured to control said multiplexer to select a correct address as said fetch address during a second period in response to said prediction check logic detecting said erroneous selection (column 6, line 59-column 7, line 30, column 16, lines 33-36).
8. Stiles et al. have not taught providing a speculative target address of a previously executed branch instruction in response to said fetch address in parallel with said instruction cache providing said line of instruction bytes. However, Gochman et al. have taught providing a speculative target address of a previously executed branch instruction in response to said fetch address in parallel with said instruction cache providing said line of instruction bytes (Gochman

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et al., Figures 3 and 4, column 4, lines 13-49) for the desirable purpose of allowing the fetch unit to continue fetching instructions without having to wait for the instruction decode, which speeds up overall execution time. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Stiles et al. provide a speculative target address of a previously executed branch instruction in response to said fetch address in parallel with said instruction cache providing said line of instruction bytes, as taught by Gochman et al., for the desirable purpose of speeding up overall execution time.

9. Referring to claim 17, Stiles et al. have taught the microprocessor of claim 16, as described above. Stiles et al. have not specifically taught wherein said second period is subsequent to said first period. However, Gochman et al. have taught wherein said second period is subsequent to said first period (Figures 3 and 4, column 4, lines 13-49) for the desirable purpose of allowing the fetch unit to continue fetching instructions without having to wait for the instruction decode, which speeds up overall execution time. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Stiles et al., include wherein said second period is subsequent to said first period, as taught by Gochman et al. (Figures 3 and 4, column 4, lines 13-49), for the desirable purpose of allowing the fetch unit to continue fetching instructions without having to wait for the instruction decode, which speeds up overall execution time.

10. Referring to claim 18, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising: instruction decode logic, configured to receive and decode said instruction bytes and to specify to said prediction check logic whether a branch

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instruction is present in said instruction bytes (column 6, line 59-column 7, line 30, column 16, lines 33-36).

11. Referring to claim 19, Stiles et al. have taught the microprocessor of claim 18, as described above, and wherein said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously comprises said prediction check logic determining that a branch instruction is not present in said instruction bytes (column 6, line 59-column 7, line 30, column 16, lines 33-36).

12. Referring to claim 20, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising: branch target address generation logic, configured to receive said line of instruction bytes and to generate an instruction pointer of an instruction comprised in said line of instruction bytes; wherein said correct address comprises said instruction pointer of said instruction (column 9, line 35-column 10, line 10).

13. Referring to claim 21, Stiles et al. have taught the microprocessor of claim 20, as described above, and wherein said instruction is comprised in said line of instruction bytes at a location of said previously executed branch instruction in said line (column 9, line 35-column 10, line 10).

14. Referring to claim 22, Stiles et al. have taught the microprocessor of claim 21, as described above, and wherein said location is cached in said BTAC (column 9, line 25-column 10, line 10).

15. Referring to claim 23, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising: branch target address generation logic, configured to receive said line of instruction bytes and to generate a correct branch target address of a branch

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instruction comprised in said line of instruction bytes based on execution of said branch instruction comprised in said line of instruction bytes; wherein said correct address comprises said correct branch target address (column 6, line 59-column 7, line 30, column 16, lines 33-36).

16. Referring to claim 24, Stiles et al. have taught the microprocessor of claim 23, as described above, and wherein said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously comprises said prediction check logic determining that said correct branch target address and said speculative target address do not match (column 6, line 59-column 7, line 30, column 16, lines 33-36).

17. Referring to claim 25, Stiles et al. have taught the microprocessor of claim 23, as described above, and wherein said branch instruction is comprised in said line of instruction bytes at a location of said previously executed branch instruction in said line (column 9, line 25-column 10, line 10).

18. Referring to claim 26, Stiles et al. have taught the microprocessor of claim 25, and wherein said location is cached in said BTAC (column 9, line 25-column 10, line 10).

19. Referring to claim 27, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising: execution logic, configured to receive said line of instruction bytes and to generate a correct direction of a branch instruction comprised in said line of instruction bytes, said correct direction generated based on execution of said branch instruction comprised in said line of instruction bytes (column 6, line 59-column 7, line 30, column 16, lines 33-36).

20. Referring to claim 28, Stiles et al. have taught the microprocessor of claim 27, as described above, and wherein said prediction check logic detecting that said control logic

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controlled said multiplexer to select said speculative target address erroneously comprises said prediction check logic determining that said correct direction indicates said branch instruction comprised in said line of instruction bytes is not taken (column 6, line 59-column 7, line 30, column 16, lines 33-36).

21. Referring to claim 29, Stiles et al. have taught the microprocessor of claim 27, as described above, and wherein said branch instruction is comprised in said line of instruction bytes at a location of said previously executed branch instruction in said line (column 9, line 25-column 10, line 10).

22. Referring to claim 30, Stiles et al. have taught the microprocessor of claim 29, as described above, and wherein said location is cached in said BTAC (column 9, line 25-column 10, line 10).

23. Referring to claim 31, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising: branch target address generation logic, configured to receive said line of instruction bytes and to generate an instruction pointer of a next instruction after an instruction comprised in said line of instruction bytes at a location of said previously executed branch instruction in said line (column 9, line 35-column 10, line 10); wherein said correct address comprises said instruction pointer of said next instruction after said instruction (column 9, line 35-column 10, line 10).

24. Referring to claim 32, Stiles et al. have taught the microprocessor of claim 31, as described above, and wherein said location is cached in said BTAC (column 9, line 25-column 10, line 10).

25. Referring to claim 33, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising:

- a. instruction decode logic, configured to receive and decode said line of instruction bytes and to specify a length of an instruction comprised in said line of instruction bytes, said instruction being at a location of said previously executed branch instruction in said line (Inherent, in order for Stiles et al. to decode the instruction, the decode logic must inherently specify the length of the instruction.).

26. Referring to claim 36, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising: instruction decode logic, configured to receive and decode said instruction and to specify which of a plurality of bytes comprising said instruction is an opcode byte (column 7, lines 57-62).

27. Referring to claim 37, Stiles et al. have taught the microprocessor of claim 36, as described above, and wherein said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously comprises said prediction check logic determining that said control logic controlled said multiplexer to select said speculative target address based on a byte of said instruction other than said opcode byte specified by said instruction decode logic (column 6, line 59-column 7, line 30, column 16, lines 33-36).

28. Referring to claim 38, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising: branch target address generation logic, configured to receive said line of instruction bytes and to generate an instruction pointer of an instruction comprised in said line of instruction bytes, said instruction located at a location of said

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previously executed branch instruction in said line; wherein said correct address comprises said instruction pointer of said instruction (column 9, line 35-column 10, line 10).

29. Referring to claim 39, Stiles et al. have taught the microprocessor of claim 16, as described above, and wherein an entry of said speculative BTAC caching said speculative target address is invalidated in response to said prediction check logic detecting said erroneous selection (column 6, line 59-column 7, line 30, column 16, lines 33-36).

30. Referring to claim 40, Stiles et al. have taught the microprocessor of claim 16, as described above, and wherein said speculative BTAC is updated with a direction prediction associated with said previously executed branch instruction, said speculative BTAC being updated in response to said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously (column 10, lines 10-15, lines 35-48).

31. Referring to claim 41, Stiles et al. have taught the microprocessor of claim 16, as described above, and wherein said speculative target address is updated in said speculative BTAC in response to said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously (column 10, lines 10-15, lines 35-48).

32. Referring to claim 42, Stiles et al. have taught the microprocessor of claim 16, as described above, and wherein said prediction check logic comprises an error output, coupled to said control logic, for notifying said control logic of said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously (column 6, line 59-column 7, line 30, column 16, lines 33-36).

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33. Referring to claim 43, Stiles et al. have taught the microprocessor of claim 16, as described above, and wherein a plurality of pipeline stages of the microprocessor are flushed in response to said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously (column 16, line 33-column 17, line 2).

34. Referring to claim 44, Stiles et al. have taught the microprocessor of claim 16, as described above, and further comprising: an instruction buffer, coupled to said instruction cache, for buffering said line of instruction bytes; wherein said instruction buffer is flushed in response to said prediction check logic detecting that said control logic controlled said multiplexer to select said speculative target address erroneously (column 16, line 33-column 17, line 2, pipeline, column 13, lines 3-47).

35. Referring to claim 45, Stiles et al. have taught the microprocessor of claim 16, as described above, and wherein said speculative BTAC and said instruction cache are accessed substantially in parallel (Stiles et al., column 9, line 35-column 10, line 10, column 2, lines 48-50).

36. Claim 60 does not recite limitations above the claimed invention set forth in claims 1-6, 10-15, 46-53, and 57-59, and 61-63 and is therefore rejected for the same reasons set forth in the rejection of claims 1-6, 10-15, 46-53, and 57-59, and 61-63 above.

37. Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiles et al., US Patent 5,163,140, in view of Gochman et al., US Patent 5,964,868 and Fite et al., US Patent 5,142,634.

38. Referring to claim 34, Stiles et al. have taught the microprocessor of claim 33, as described above. They have not specifically taught wherein said prediction check logic detecting

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that said control logic controlled said multiplexer to select said speculative target address erroneously comprises said prediction check logic determining that said length of said instruction does not match an instruction length cached in said speculative BTAC for said previously executed branch instruction. However, Fite et al. have taught prediction check logic is configured to determine if said first instruction length does not match a second instruction length that is cached in the BTAC and received therefrom (Fite et al., column 16, line 27-62, column 21, lines 14-15, column 24, lines 9-26, column 27, lines 9-24) for the desirable purpose of determining whether the address of the branch instructions has a valid associated entry in the cache. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the branch control logic of Stiles et al. notify said branch control logic that the microprocessor erroneously branched to the speculative target address, using the instruction length comparison concept, as taught by Fite et al., for the desirable purpose of determining branch speculation validity (Fite et al., column 16, line 27-62, column 21, lines 14-15, column 24, lines 9-26, column 27, lines 9-24).

39. Referring to claim 35, Stiles et al. have taught the microprocessor of claim 34, as described above, and further comprising: branch target address generation logic, configured to receive said instruction and to generate an instruction pointer of said instruction; wherein said correct address comprises said instruction pointer of said instruction (column 9, line 35-column 10, line 10).

Response to Arguments

40. Applicant's arguments with respect to claims 16-45 and 60 have been considered but are moot in view of the new ground(s) of rejection.

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41. Applicant's arguments filed December 17, 2004 with respect to claims 1-15, 46-59, and 61-63 have been fully considered but they are not persuasive.

42. On page 17, Applicant argues in essence:

“Applicant can find no teaching in Stiles of the microprocessor branching to a predicted target address provided by the BPC of Stiles until decoding the instruction and therefore knowing that the instruction pointed to by the decode PC use to make the target address is a branch instruction.”

It is unclear as to what Applicant is specifically arguing as the sentence is incomprehensible. It appears that Applicant is attempting to argue that Stiles et al. have not taught “a storage element, for storing an indication of whether the microprocessor branched to the speculative target address provided by the BTAC without knowing whether an instruction associated with said instruction is a branch instruction”. However, Stiles et al. has in fact taught this claimed storage element. This indication must inherently be stored so that instructions that have been incorrectly speculatively executed can be corrected (column 16, line 32-column 17, line 27). If this indication was not stored then Stiles et al. would not know which instructions to delete and/or restore to return the processor to the appropriate state to continue correct instruction processing. Therefore this argument is moot.

43. On page 17, Applicant argues in essence:

“Stiles does not teach the tag indicating whether the microprocessor branched to a predicted target address provided by the BPC without knowing whether an instruction associated with the indication is a branch instruction, much less handling an exception condition associated with such a condition.”

Applicant is arguing a feature of the invention not specifically stated in the claim language, which is improper. Claimed subject matter, not the specification, is the

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measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Self*, 213 USPQ 1,5 (CCPA 1982); *In re Priest*, 199 USPQ 11,15 (CCPA 1978).

"It is the claims that measure the invention." *SRI Int'l v. Matshshita Elec. Corp.*, 775 F.2d 1107, 1121, 227 USPQ 577, 585 (Fed. Cir. 1985) (en banc).

"The invention disclosed in Hiniker's written description may be outstanding in its field, but the name of the game is the claim." *In re Hiniker Co.*, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

"[A]s an initial matter, the PTO applies to the verbiage of the proposed claims the broadest reasonable meaning of the words in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description contained in the applicant's specification." *In re Morris*, 44 USPQ2d 1023, 1027 (Fed. Cir. 1997).

"limitations appearing in the specification will not be read into the claims, and ... interpreting what is meant by a word in a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper'." *Intervet Am., v. Kee-Vet Labs.*, 12 USPQ2d 1474, 1476 (Fed. Cir. 1989) (citation omitted).

"it is entirely proper to use the specification to interpret what the patentee meant by a word or phrase in the claim, ... this is not to be confused with adding an extraneous limitation appearing in the specification, which is improper. By 'extraneous,' we mean a limitation read into a claim from the specification wholly apart from any need to interpret ... particular words or phrases in the claim." *In re Paulsen*, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994) (citation omitted).

In this case, Applicant has not specifically claimed a *"tag indicating whether the microprocessor branched to a predicted target address provided by the BPC without knowing whether an instruction associated with the indication is a branch instruction."*

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This limitation is not read into the claims for the purpose of avoiding the prior art.

Therefore this argument is moot.

44. On page 17, Applicant argues in essence:

“Although the Examiner cites text in Stiles that a predicted address is not guaranteed to be correct and must eventually be checked elsewhere within the CPU, this text does not teach branching to the BPC-predicted target address without knowing whether the instruction was a branch instruction, but only teaches that the predicted address may be incorrect, for example because it is the target address of some other branch instruction whose lower address bits map to the same entry in the direct-mapped, tagless second level BPC. Col. 17, lines 22-25.”

However, Applicant is directed to Stiles et al., specifically column 9, lines 58-62 and column 16, line 59-column 17, line 27. A look-up in the second level branch prediction cache is always assumed to hit for all instructions. Therefore, finding an instruction to be incorrectly predicted includes the case of finding an instruction, that is not a branch instruction, which causes the instruction to be incorrectly predicted. So, when a non-branch instruction is incorrectly predicted as a taken branch and then subsequently executed, the system is eventually restored to an appropriate state from which to continue processing. Stiles et al. have in fact taught branching to the BPC-predicted target address without knowing whether the instruction was a branch instruction (column 9, lines 58-62 and column 16, line 59-column 17, line 27). Therefore this argument is moot.

Conclusion

45. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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46. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

47. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

48. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

49. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm


RICHARD L. ELLIS
PRIMARY EXAMINER